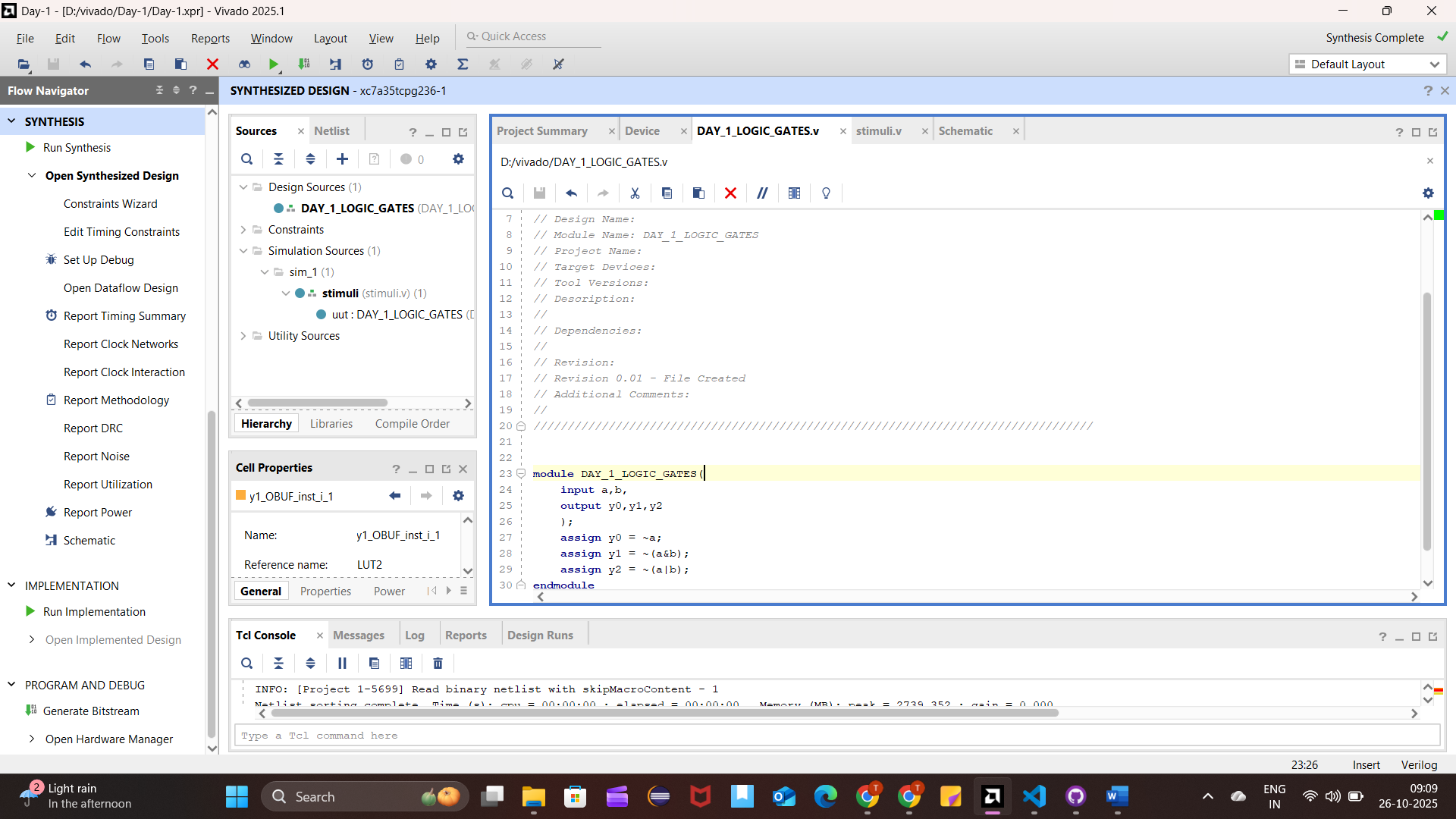
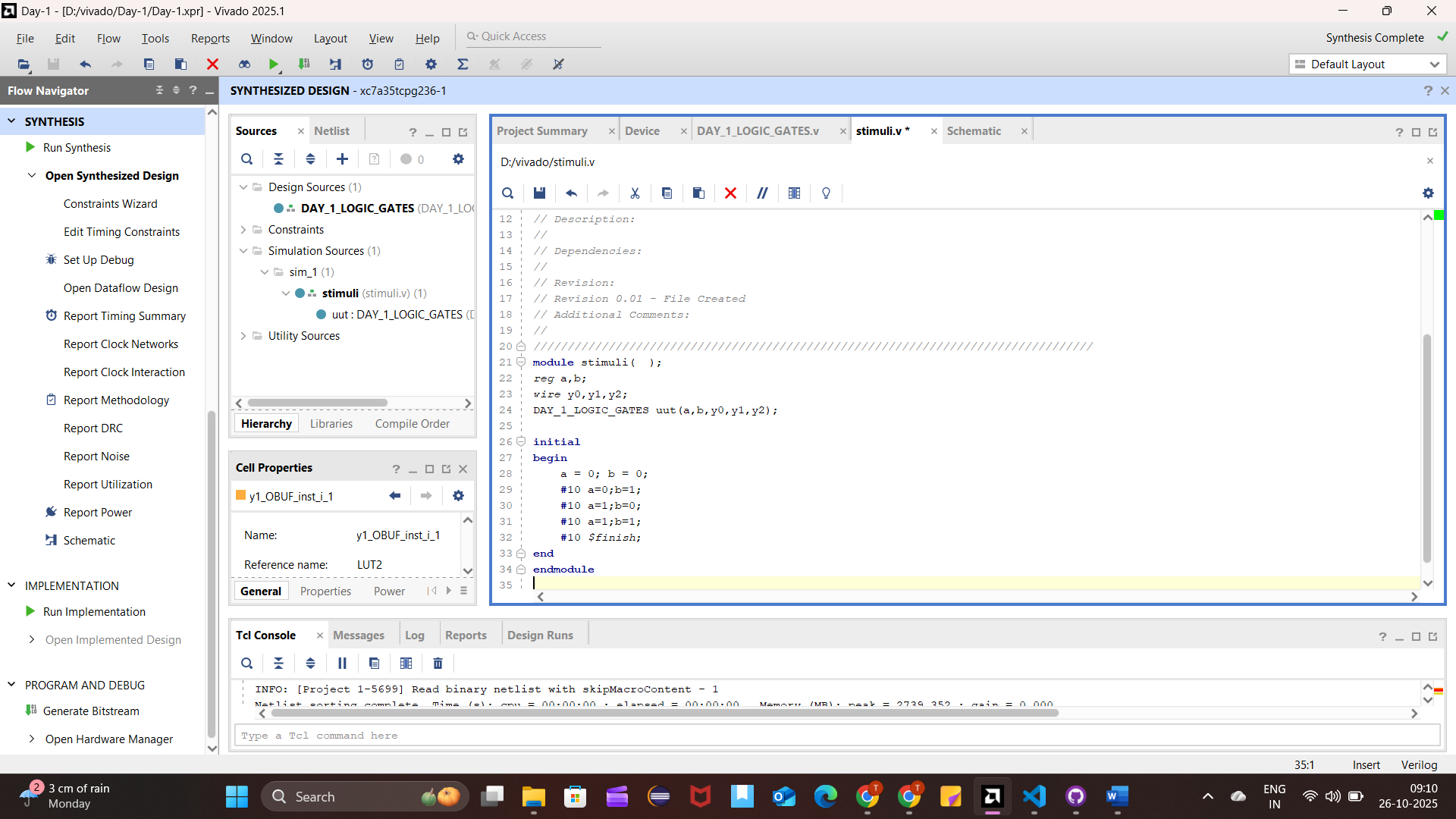
Day 1

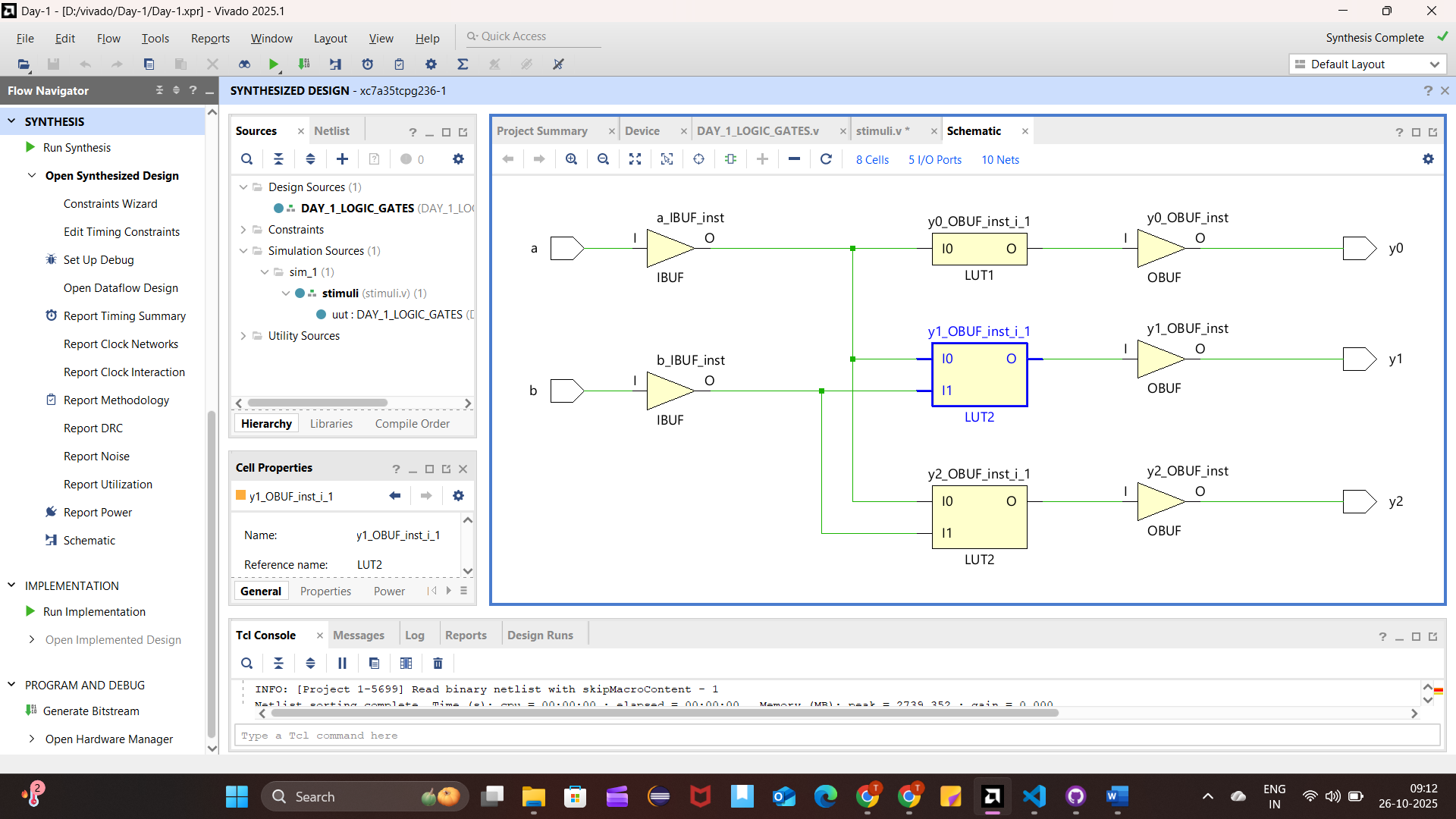
Design sources



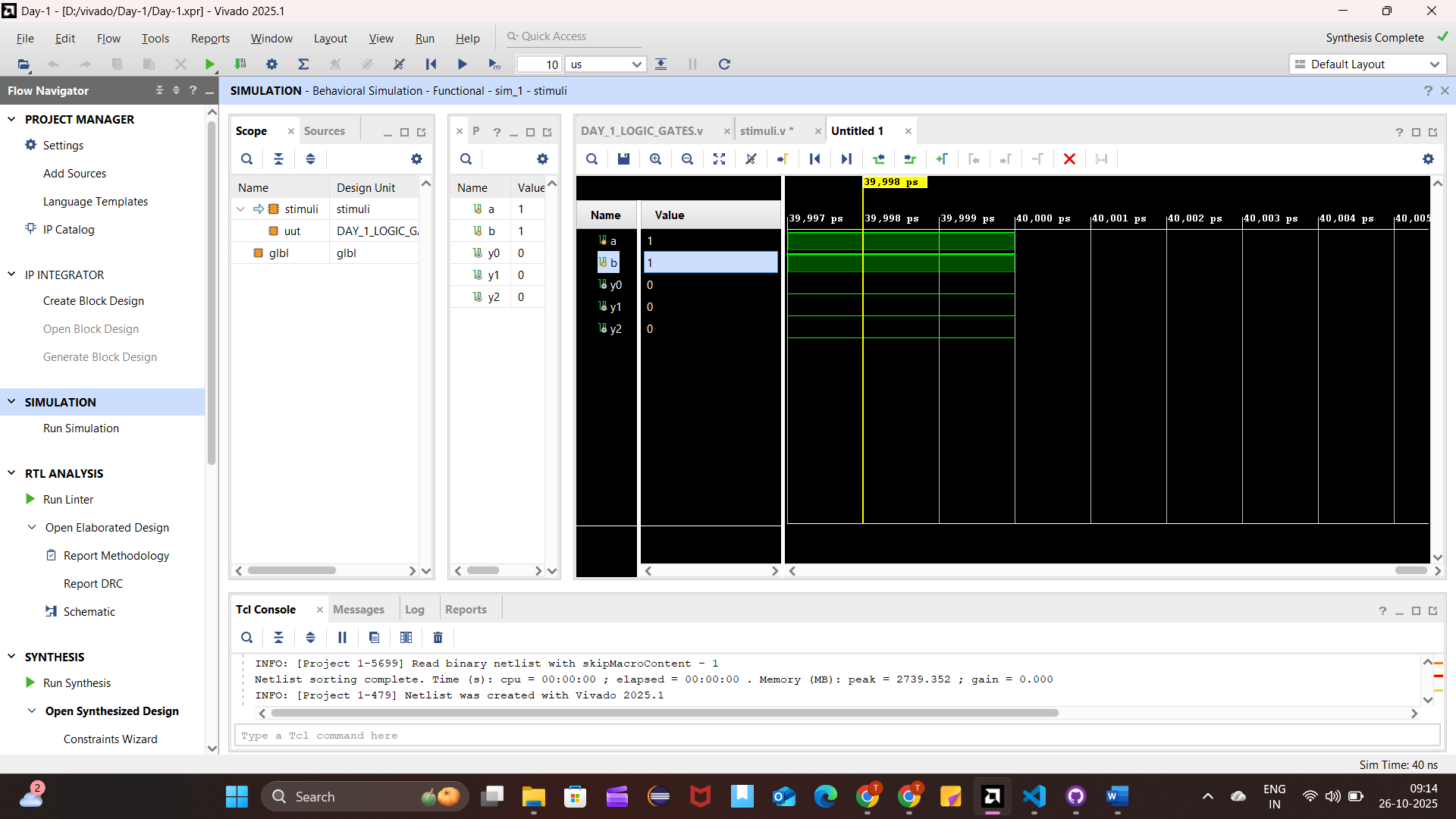
Stimulating sources



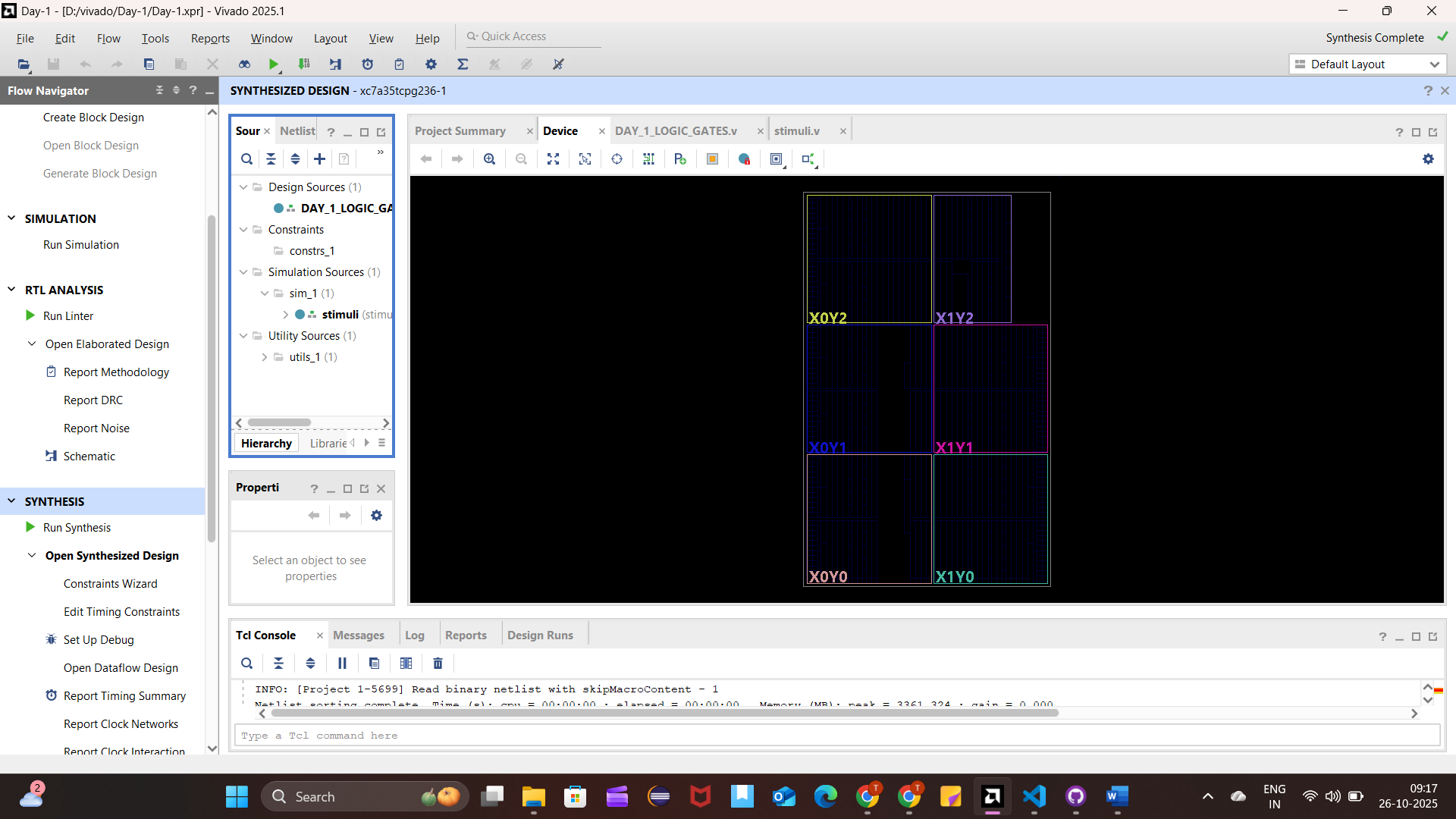
Schematic design of logic gates



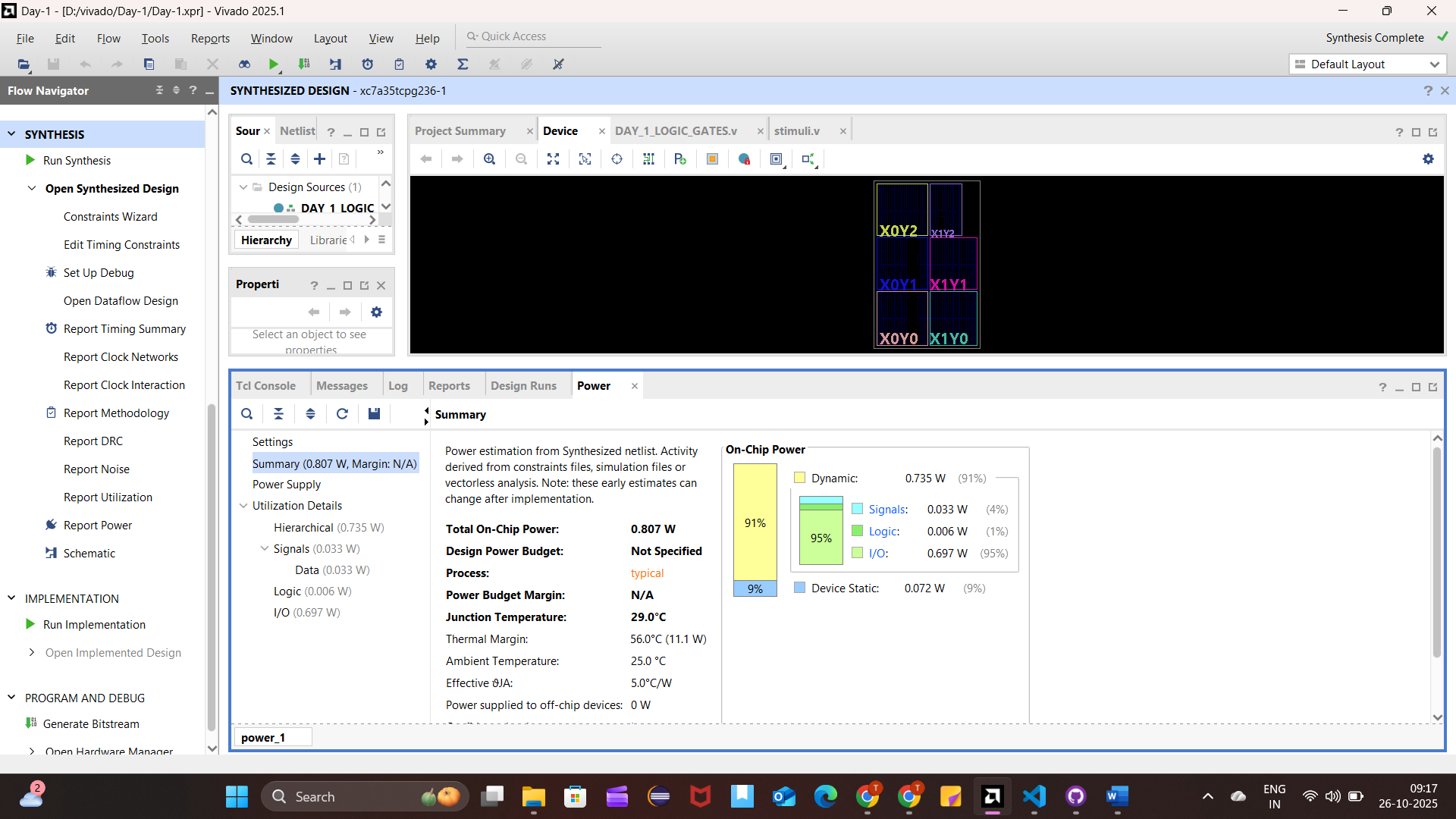
Run simulation output:



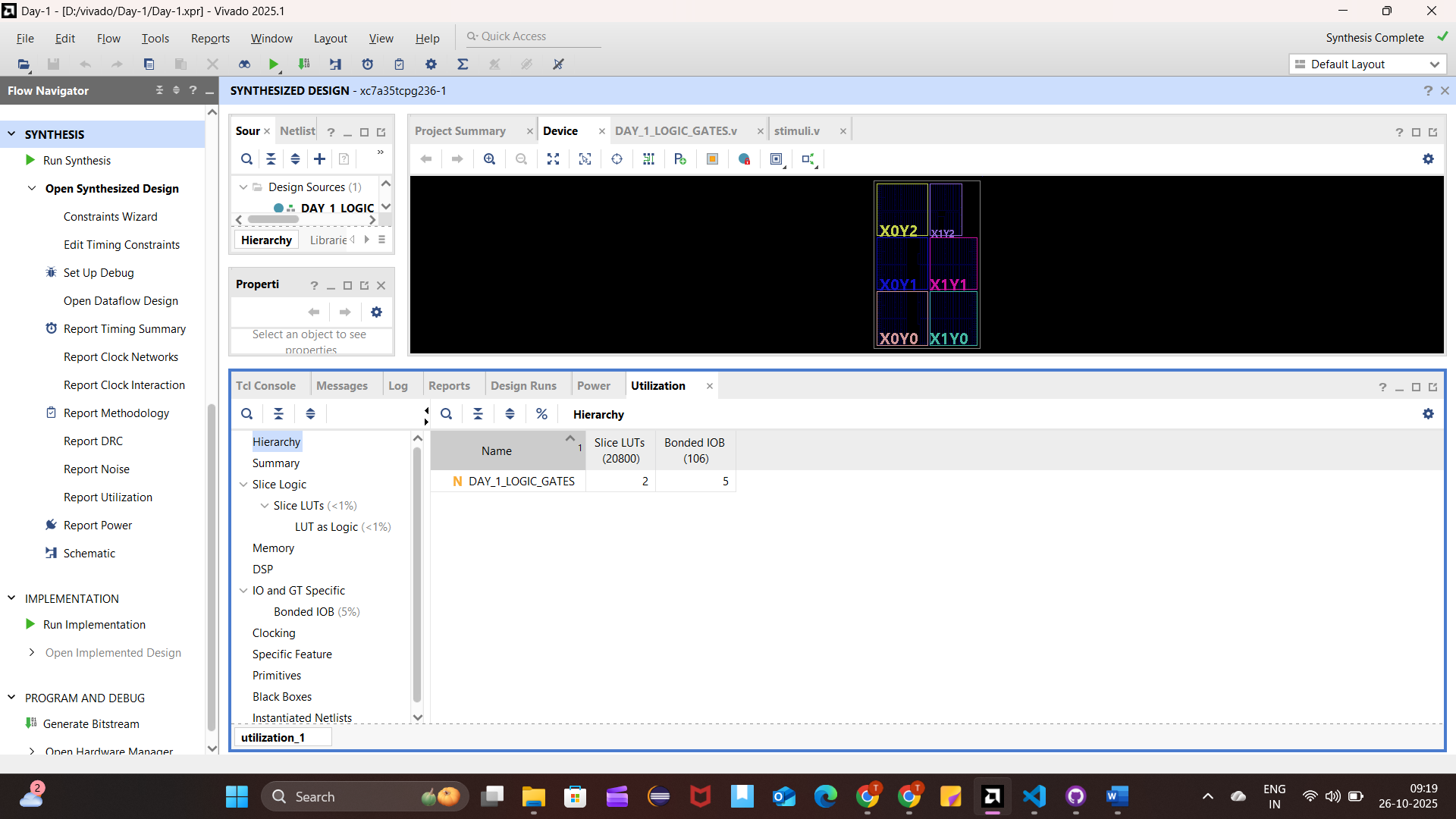
Synthesized design



Power report



Utilization report



Project summary

